

Integration Methods for High-Density Integrated Electric Drives

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Overview

Timeline

- Start Date: *April 2019*
- End Date: *March 2024*
- Percent Complete: 60%

Budget

- Total project funding: *\$1.5 million*
- Funding for FY22: *\$300,000*
- Funding for FY23: *\$300,000*

Barriers & Technical Targets

Single-chip gate drive: low-voltage, high-temperature (>200°C) sic fabrication process; achieves 40-50% PCB volume savings

Power modules: proven techniques for heterogeneously integrated power module (>200°C)

Sensing: highly compact, high temperature, noise immune, high bandwidth (>100 MHz) current sensing

Partners

- Oak Ridge National Laboratory
- Virginia Tech
- Stony Brook University

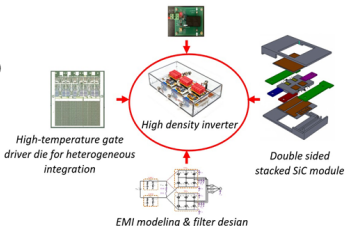
Approach / Strategy

Goal

The research work performed by the UA towards the primary objective involves integrated circuit design, sensor evaluation, and power electronic module packaging tasks.

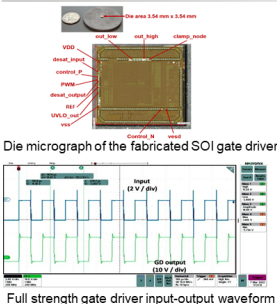
Integration Motivation

- Smaller circuit parasitics (lower gate and power loop inductance) for increased efficiency
- Higher power density
- Higher temperature operation
- Less aggressive cooling technique
- Better control, EMI
- Ultimately, higher reliability



Technical Accomplishments – FY22

Takeaway: Successful Tape-out on SOI Process and Gate Driver Die Evaluation

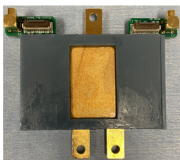


Pad name	Description and test condition	
VDD	Positive power supply	→15 V
REF	Reference voltage	→ 0 V
VSS	Negative power supply	→ -3 V
PWM	Input signal	→ -3 V to 0 V
Load	16 nF	
(out_low and out_high shorted)	(representation of two CREE cpm3-1200-0013a SiC power die placed in parallel in a switching position)	
control_P	Pull-up drive strength control pin	→ set to 0 V
control_N	Pull-down drive strength control pin	→ set to 0 V
Output	- 3 → 15 V	
Parameters	Tested at 25 °C	Tested at 175 °C
Rise time	401 ns	442 ns
Fall time	350 ns	382 ns
Average propagation delay	287 ns	318 ns

Technical Accomplishments – FY22

Takeaway: Fabrication of Gen1b Modules

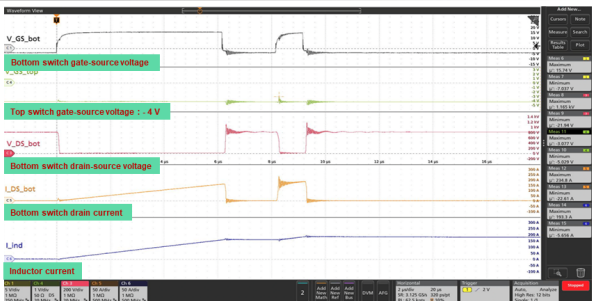
Specification	Value
Number of paralleled devices	Two
Key integrated parts (mm)	Two gate driver boards (53.92*26.14*12.12 each)
Dimension without gate driver boards (mm)	76.5*41.4*5.51
Dimension with gate driver boards (mm)	76.5*89.25*15.78
Voltage (V)	1200
Current (A)	164 @ T _j =160°C
Power loop inductance (nH)	4.97
Gate loop inductance (nH)	15



Six power modules for a segmented two-level three-phase inverter are fabricated and tested

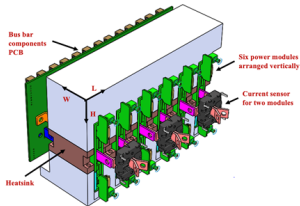
Technical Accomplishments – FY22

Takeaway : Double Pulse Test up to 800 V, 164 A with Gen1b Power Module



Technical Accomplishments – FY22

Takeaway : Motor Drive Assembly Design and Integration with Fabricated Modules

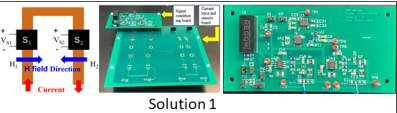


Overall inverter volume with Gen1b module	2.59 L
Peak power rating	200 KW

Technical Accomplishments – FY22

Takeaway : Two GMR Sensors (TGS) Method Test and Evaluation

Two GMR sensors (TGS) method for increasing the resolution of the current measurement system and decreasing the errors of the measurement at different temperatures



Solution 1: Placing sensors on a U shape trace

Solution 2: Locating sensors on two sides of the trace (plane)

Collaboration and Coordination with Other Institutions

Virginia Tech

- Design of double-side cooled power module with DBC/IMS
- Processing and characterization of sintered-metal interconnect
- Packaging of high-temperature gate driver



Oak Ridge National Laboratory

- High performance liquid cooled heat sink design
- Insulated metal substrate development for single and double sided packaging
- System integration and evaluation



Stony Brook University

- Experiment and modeling investigation of integrated current sensing solutions



Summary

Technical Accomplishments

- Successful tape-out on SOI process and gate driver die evaluation
- Fabrication of Gen1b Modules
- Double pulse test up to 800 V, 164 A with fabricated double-sided stacked Gen1b power module
- Motor Drive Assembly Design and Integration with Fabricated Modules
- Two GMR Sensors (TGS) method test and evaluation

Proposed Future Work – FY 23

- To design, fabricate and test the next version of modified high-temperature integrated circuits based on the design analysis and test results obtained from this fabrication run.
- To design integrated power module with all the possible integration solutions studied for gate driver, decoupling capacitors, current and temperature sensors
- To design and validate second version of the TGS method for increased resolution and decreased sensitivity to temperature fluctuations

** Any proposed future work is subject to change based on funding levels.